

WHAT IS CLAIMED IS:

1 1. A semiconductor device comprising:
2 an insulator layer;
3 a planar transistor formed on a first portion of a semiconductor layer, the first portion of
4 the semiconductor layer overlying the insulator layer, and the first portion of the semiconductor
5 layer having a first thickness; and
6 a multiple-gate transistor formed on a second portion of the semiconductor layer, the
7 second portion of the semiconductor layer overlying the insulator layer, the second portion of the
8 semiconductor layer having a second thickness, and the second thickness being larger than the
9 first thickness.

1 2. The semiconductor device of claim 1, wherein the semiconductor layer comprises a
2 material selected from a group consisting of silicon, germanium, silicon germanium, and
3 combinations thereof.

1 3. The semiconductor device of claim 1, wherein the insulator layer comprises silicon oxide.

1 4. The semiconductor device of claim 1, wherein the first thickness is less than about 400
2 angstroms.

1 5. The semiconductor device of claim 1, wherein the second thickness is greater than about
2 100 angstroms.

1 6. The semiconductor device of claim 1, wherein the planar transistor comprises:
2 a planar channel formed from the first portion of the semiconductor layer;

3 a gate dielectric overlying at least a portion of the planar channel;
4 a gate electrode overlying the gate dielectric; and
5 source and drain regions formed in the first portion of the semiconductor layer oppositely
6 adjacent the gate electrode.

1 7. The semiconductor device of claim 6, wherein the gate dielectric comprises a material
2 selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a
3 dielectric with a relative permittivity larger than about 5, and combinations thereof.

1 8. The semiconductor device of claim 6, wherein the gate electrode comprises a material
2 selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline
3 silicon, and combinations thereof.

1 9. The semiconductor device of claim 1, wherein the multiple-gate transistor comprises:
2 a vertical semiconductor fin formed from the second portion of the semiconductor layer;
3 a gate dielectric at least partially wrapping around a channel portion of the fin;
4 a gate electrode overlying the gate dielectric; and
5 source and drain regions formed in the second portion of the semiconductor layer
6 oppositely adjacent the gate electrode.

1 10. The semiconductor device of claim 9, wherein the gate dielectric comprises a material
2 selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a
3 dielectric with a relative permittivity larger than about 5, and combinations thereof.

1 11. The semiconductor device of claim 9, wherein the gate electrode comprises a material
2 selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline
3 silicon, and combinations thereof.

1 12. The semiconductor device of claim 1, wherein corners of the semiconductor layer are
2 rounded at edges of active regions of the planar and multiple-gate transistors.

1 13. A semiconductor device comprising:

2 an insulator layer;

3 a first portion of a semiconductor layer having a first thickness, the first portion of the

4 semiconductor layer overlying the insulator layer;

5 a second portion of the semiconductor layer having a second thickness, the second

6 portion of the semiconductor layer overlying the insulator layer, and the second thickness being

7 larger than the first thickness;

8 a first transistor having a first active region formed from the first portion of the

9 semiconductor layer; and

10 a second transistor having a second active region formed from the second portion of the

11 semiconductor layer.

1 14. The semiconductor device of claim 13, wherein the first thickness is less than about 400

2 angstroms, and the second thickness of greater than about 100 angstroms.

1 15. The semiconductor device of claim 14, wherein the first transistor is a planar transistor,

2 and the second transistor is a multiple-gate transistor.

1 16. The semiconductor device of claim 13, wherein corners of the first and second active

2 regions are rounded.

- 1 17. A semiconductor device comprising:
 - 2 an insulator layer;
 - 3 a first portion of the semiconductor layer having a first thickness of less than about 400
 - 4 angstroms, the first portion of the semiconductor layer overlying the insulator layer;
 - 5 a second portion of the semiconductor layer having a second thickness of greater than
 - 6 about 100 angstroms, the second portion of the semiconductor layer overlying the insulator layer,
 - 7 and the second thickness being larger than the first thickness;
 - 8 a first transistor having a first active region formed from the first portion of the
 - 9 semiconductor layer; and
 - 10 a second transistor having a second active region formed from the second portion of the
 - 11 semiconductor layer.
- 1 18. The semiconductor device of claim 17, wherein the first transistor is a planar transistor,
 - 2 and the second transistor is a multiple-gate transistor.

1 19. A method of fabricating a semiconductor device comprising:

2 forming a first thickness of a first portion of a semiconductor layer, and a second

3 thickness of a second portion of the semiconductor layer larger than the first thickness, wherein

4 the semiconductor layer is overlying an insulator layer;

5 forming a first active region for a first transistor from the first portion of the

6 semiconductor layer; and

7 forming a second active region for a second transistor from the second portion of the

8 semiconductor layer.

1 20. The method of claim 19, wherein the forming of the first and second active regions

2 comprises:

3 providing a patterned active region mask over the semiconductor layer; and

4 removing material from the semiconductor layer in alignment with the active region mask

5 to form the first active region in the first portion and to form the second active region in the

6 second portion.

1 21. The method of claim 19, wherein the first transistor is a planar transistor and wherein the

2 second transistor is a multiple-gate transistor.

1 22. The method of claim 19, further comprising:

2 forming a first gate dielectric over a first channel region of the first active region;

3 forming a first gate electrode over the first gate dielectric;

4 doping portions of the first active region to form source and drain regions for the first

5 transistor;

6 forming a second gate dielectric over a second channel region of the second active

7 region;

8 forming a second gate electrode over the second gate dielectric; and

9 doping portions of the second active region to form source and drain regions for the

10 second transistor.

1 23. The method of claim 22, wherein at least part of the doping of the first and second active

2 regions is performed after the forming of the first and second gate electrodes.

1 24. The method of claim 22, wherein at least part of the doping of the first and second active

2 regions is performed before the forming of the first and second gate electrodes.

1 25. The method of claim 22, wherein the first and second gate dielectrics are formed from a

2 same material.

1 26. The method of claim 22, wherein the first and second gate electrodes are formed from a

2 same material.

1 27. The method of claim 19, wherein the semiconductor layer comprises silicon, and wherein

2 the forming of the first thickness of the first portion of the semiconductor layer comprises:

3 providing a patterned mask that covers at least part of the second portion and is open over

4 at least part of the first portion;

5 oxidizing an exposed top portion of the first portion to form silicon oxide;

6 removing the silicon oxide; and

7 removing the mask.

1 28. The method of claim 19, wherein the forming of the first and second active regions is
2 performed after the removing of the part of the first portion to provide the first thickness of the
3 first portion.

1 29. The method of claim 19, wherein the forming of the first and second active regions is
2 performed before the removing of the part of the first portion to provide the first thickness of the
3 first portion.

1 30. The method of claim 19, wherein the second active region is a fin with a fin height of
2 more than about 100 angstroms and a fin width of less than about 500 angstroms.

1 31. The method of claim 19, wherein the second active region is a fin with a fin height of
2 more than about 400 angstroms and a fin width of less than about 500 angstroms.

1 32. The method of claim 19, wherein the forming of the first and second active regions
2 comprises:
3 forming an active region mask to expose selected regions of the first and second portions;
4 and
5 forming trenches in the selected regions to define the first and second active regions.

1 33. The method of claim 32, further comprising:
2 filling the trenches with a dielectric material; and
3 removing the active region mask.

1 34. The method of claim 19, wherein the semiconductor layer comprises a material selected
2 from a group consisting of silicon, germanium, silicon germanium, and combinations thereof.

- 1 35. The method of claim 19, further comprising:
 - 2 forming rounded corners on the first and second active regions.

- 1 36. The method of claim 35, wherein at least some of the rounded corners have a radius of
 - 2 curvature between about 10 angstroms and about 200 angstroms.

- 1 37. The method of claim 35, wherein the forming of the rounded corners is performed using
 - 2 an anneal in a hydrogen-containing ambient with a pressure between about 5 and about 20 Torr,
 - 3 for a duration of between about 15 and about 35 seconds, at a temperature between about 800
 - 4 and about 1000 degrees Celsius.